Power and Reliability Analysis for Next Generation Integrated Fan-out Wafer-Level Packaging

ANSYS

ABSTRACT

This talk will focus on the emerging Fan-out Wafer-level Packaging that quickly caught Mobile designers' attention as the package for next generation mobile devices. However, the irregular interconnect layers of the new package demands accurate extraction and power/signal EM analysis which are not required on traditional packages. With multiple dies on wafer-level package, power/reliability analysis needs to consider the noise coupling from dies and package itself. ANSYS provides complete solution for power/reliability/SI/EMI analysis of IC packages.

ANSYS

Power and Reliability Analysis for Next Generation Integrated Fan-out Wafer-Level Packaging

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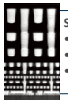
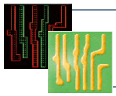
TSMC OIP 2016

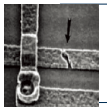
N10/N7 RedHawk/Totem Foundry Certification



Support Unique Metal Architecture
- Special metal layers and color-based R/C extraction
- Complex via structures and shapes
- Diffusion as interconnect structures



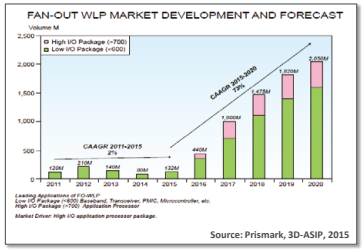
Enhanced Modeling
- Dummy devices
- Vertical resistance
- Double patterning

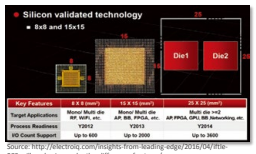


Complex EM, ESD, Self-heat support
- Current-direction, metal topology based
- Color-based EM rule and special handling
- Layout-based selfheat and thermal coupling among wires
- Pseudo-via, RMS thermal-aware EM

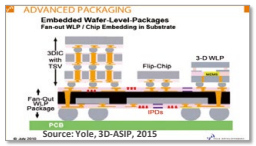
- **Color-aware Resistance Calculation**
- **Handling Bridge-via and SRAM Coloring**
- **Color-aware EM Rule Handling**
- **IR/EM Extraction and Analysis**
- **Layout-based Self-heat Analysis including Thermal Coupling among Wires**

Market Trend of Fan-out Wafer-level Packaging





Source: http://electroiq.com/insights-from-leading-edge/2016/04/iftle-283-will-packaging-make-the-difference-for-tsmc/



Form Factor
Smaller form factor requirements
Mobile applications

Performance
Higher bandwidth requirements
Memory/SoC stack

Cost
High cost sensitivity
Especially in mobile applications

Advantages of Wafer Level Packaging (TSMC InFO)

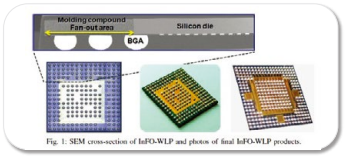
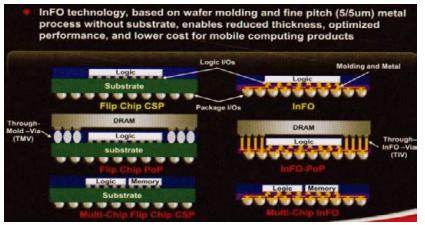


Fig. 1. SEM cross-section of InFO-WLP and photos of final InFO-WLP products.

	FC-BGA/MCM	InFO-WLP
Package Size (mm²)	8x8	
Die Size (mm²)	1-5x5 die, 2-2x1.25 dies	
Die Thickness (mm)	0.5	<0.3
Substrate Thickness (mm)	0.3	N/A
Ball Count	400	
Ball Diameter/Pitch (mm)	0.26/0.4	
Total Power (W)	2.0	
Ambient Temp (°C)	25	
Max Temp (°C)	90.5	81.5
Thermal Resistance (°C /W)	32.5	28.0

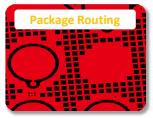
Table 1: Simulation conditions for thermal analysis from IEEE TSMC InFO paper, IEDM 2012



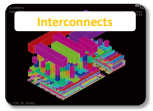
http://electroiq.com/insights-from-leading-edge/2016/04/iftle-283-will-packaging-make-the-difference-for-tsmc/

- Reduction in die thickness
- Lower maximum temperatures
- Lower cost for mobile applications

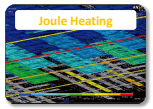
Special Power & Reliability Analysis Requirements



- Irregular package geometries
- Special handling for accurate RLC extraction and EM rules



- Complex interconnect geometries
- Need to consider interaction between package and die metal layers

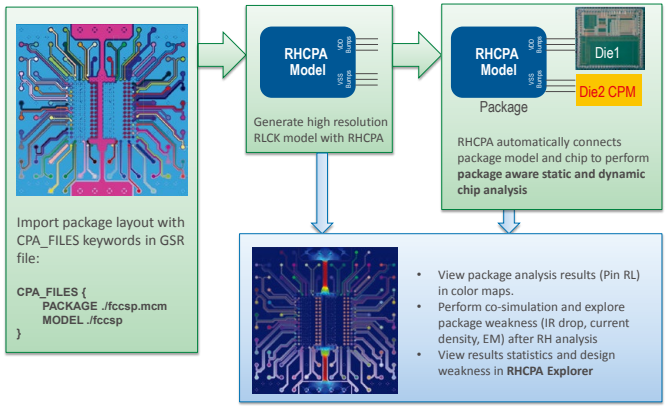


- Thermal integrity for shared package between multiple dies
- Need for EMI and SSO analysis

Approaches to Multi-die Power Integrity Analysis

- **Multi Die Analysis Using RedHawk Chip-Package-Analysis**
  - Package layers imported as mcm file
  - Die analysis using 2nd die as a CPM model, with both die and package layers co-visualizable
  - Static/EM and dynamic analysis performed on chips and package layers
- **Multi Die Analysis Using RedHawk 3DIC for InFO**
  - Package layers imported as GDS
  - Multi-die concurrent analysis using detailed data for all dies
  - Static/Dynamic/EM analyses performed on chips and package layers

Multi-die Power/Reliability Flow with RedHawk-CPA

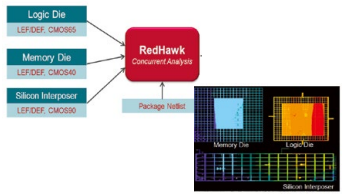


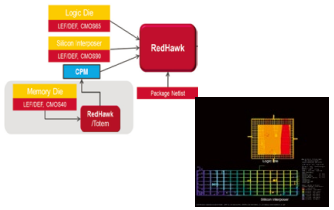
Enabling 2.5D/3D IC Designs for PI Analysis in RedHawk-3DIC for InFO

- **Shared P/G network in multiple dies in WLP or 3D-IC designs**
- **Need simultaneous multi-die simulation or model based analysis for noise propagation among dies/package**

Concurrent analysis
- Full-layout visibility of all IC/WLP/Interposer
- hierarchical capacity

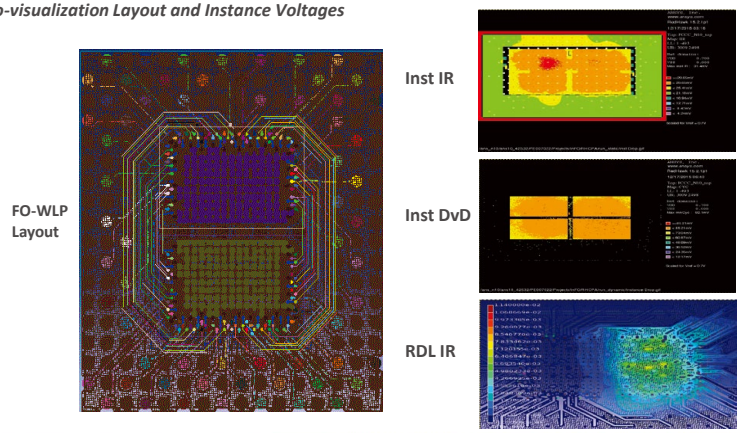
Model based analysis
- Inclusion of CPM for some dies
- WLP/interposer modeling



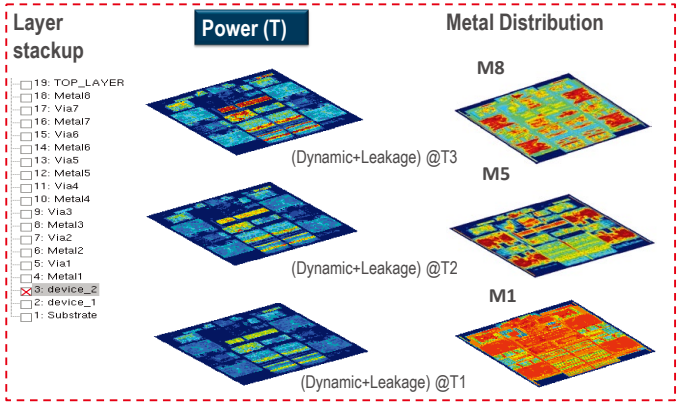


Static IR/Dynamic Noise on an Example FO-WLP

Co-visualization Layout and Instance Voltages



Chip Thermal Model (CTM) from RH/Totem

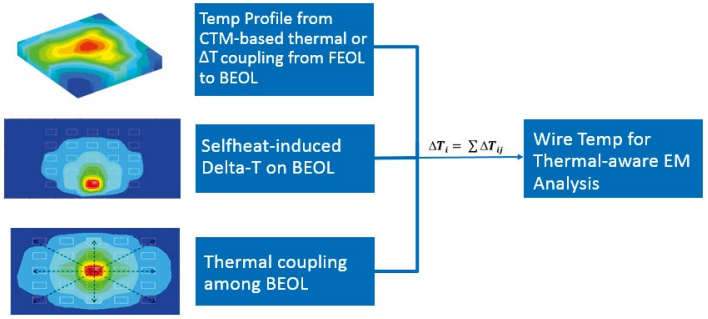


CTM content

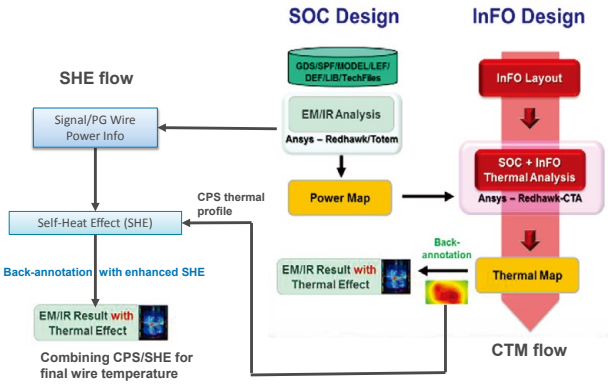
- Layer Stackup
- Temp-dependent tile-based power density maps
- Per layer metal density map

Device and Wire Delta-T Flow

Including Thermal Coupling among Wires (PG and Signal Wires)



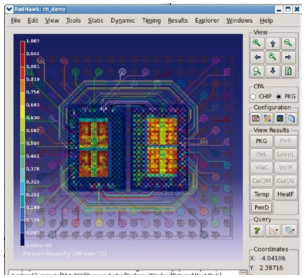
InFO Thermal Reference Flow



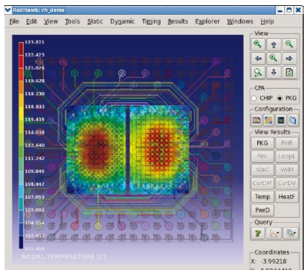
RH-CTA: Chip Power/Thermal Profiles on InFO with Two SoC Dies

CTM-based InFO thermal analysis with Chip-Package-System

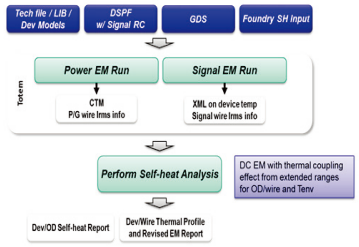
Power Density



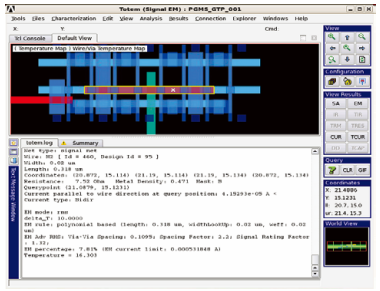
Temperature



InFO CTM-based Thermal Analysis Combined with Selfheat DC EM Flow



Combining CTM-based InFO Thermal Analysis with Selfheat DC EM Flow



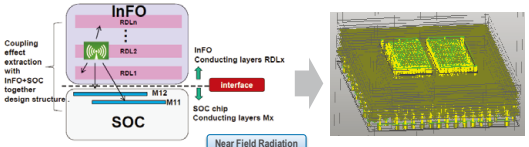
Temperature Map on Wire-level Resolution

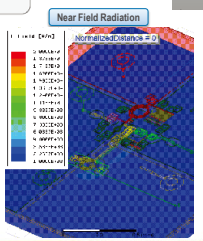
ANSYS Solution: Power/Signal/EMI/Thermal Analysis

Fan-out Wafer-level Package

WLP analysis for Power, Signal, Thermal and EMI analysis

- Model coupling effects of InFO and SoC
- Simulate combined PI/SI/Thermal/EMI effects

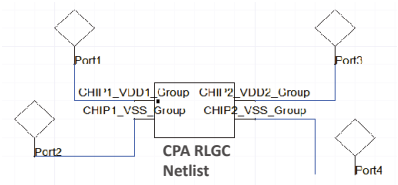




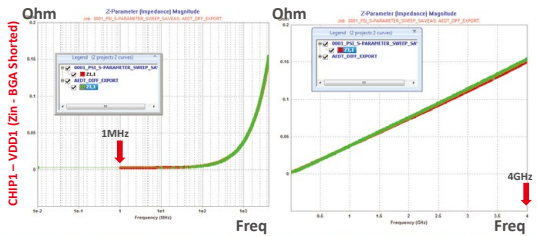
ANSYS Solutions:

- ✓ **ANSYS CPM/CPA**: Resonant analysis, Q factor, Z profile, current density, IR drop on InFO package
- ✓ **ANSYS SIwave**: S-parameter, SPICE model export for SSO
- ✓ **ANSYS SIwave/HFSS:** Far-field, Near-field (E and/or H)
- ✓ **ANSYS SIwave/IcePak:** Electrical-Thermal two-way coupling

Results Comparison over 100MHz - 4GHz between SIwave-CPA and SIwave-PSI/HFSS



- CPA generates an RLCG netlist, that is converted to S-parameters
- Ports created on CHIP1 and CHIP2 converted to differential S-parameters by sweeping frequency from 100MHz to 4GHz
- SIwave-PSI performs 3D full-wave FEM solving

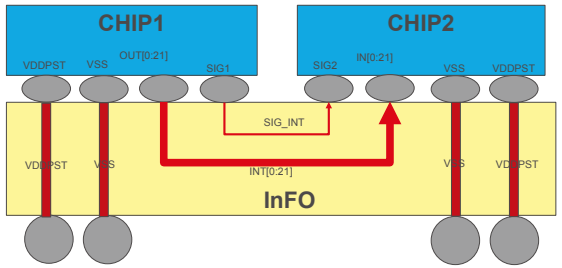


RED: 3D Full-wave FEM Solver
GREEN: CPA Model

Loop Inductance: CHIP1 VDD1

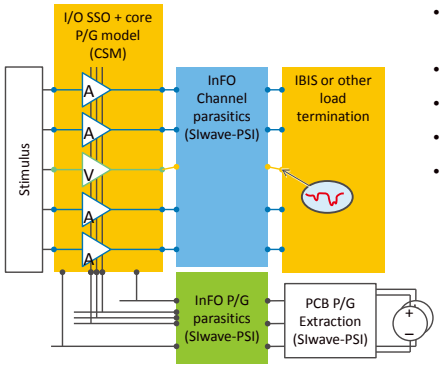
Freq	3D Full-wave PSI Solver	CPA RLCG
100MHz	6.15pH	6.23pH (1.3%)
1GHz	5.84pH	6.02pH (3%)
4GHZ	5.95pH	6.14pH (3.1%)

InFO SSO Analysis: Enables InFO Channel Communication with Quality Eye Opening



- CHIP1 SIG1 → InFO SIG_INT → CHIP2 SIG2
- CHIP1 OUT[0:21] → InFO INT[0:21] → CHIP2 IN[0:21]
- VDDPST & VSS for P/G

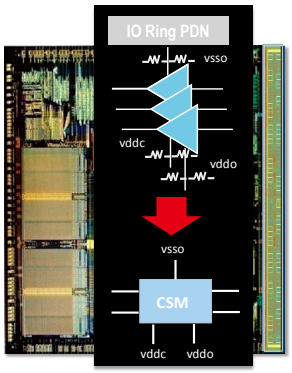
InFO SSO Analysis



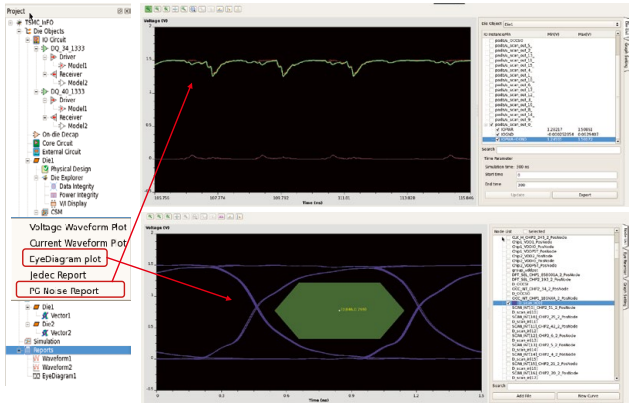
- SoC drivers and receivers + core noise modeled in CSM
- InFO rails, signals nets, passives
- IBIS or transistor model
- Stimulus
- With CIOM (Compact IO Model) for fast transient simulation

Chip Signal Model (CSM) : Chip IO Model (CIOM) + Reduced IO Ring PDN Model

- **Chip IO Model (CIOM)**
  - Non-linear device macro-model for IO cells
  - Spice level accuracy with full IO bank simulation capacity
  - Model impact of P/G noise
  - Allows protection of underlying IP
  - Order of magnitude reduction in elements from transistor model
- **Reduced IO Ring PDN Model**
  - Multiple PG nets
  - Signal nets
  - Implicit inclusion of intentional decoupling capacitance
  - Orders of magnitude reduction in elements from original extraction

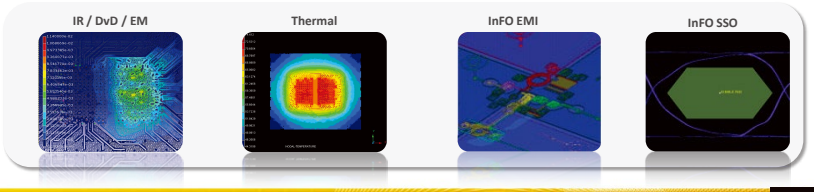


SSO P/G Noise and Eye Diagram View on InFO Case



Summary: Power and Reliability Analysis for InFO
Multi-die Power, Thermal, EMI, and SSO Analysis

- Multi-die power integrity analysis w/ concurrent or model-based methods
- Extraction/EM engines enhanced to handle InFO IR/EM accuracy
- 3DIC thermal integrity analysis w/ CTM-based method and detailed selfheat
- Wire, TSV and BGA can be thermally modeled in details
- Comprehensive PI/SI analysis
- EMI and SSO analysis performed on multi-die InFO design



ANSYS Multi-Physics Simulation for CPS Design with Chip Models